26

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/490,263	01/24/2000	Jing Wang		6937

7590 01/02/2003

KLEIN O'NEILL & SINGH
2 PARK PLAZA
SUITE 510
IRVINE, CA 92614

EXAMINER	
HUYNH, KIM T	
ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 01/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/490,263	Applicant(s) WANG ET AL.	
	Examiner Kim T. Huynh	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 January 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Notice to Applicant(s)

1. This application has been examined. Claims 1-59 are pending.

Response to Amendments

2. Applicant's amendment filed 10/07/02 with respect to claims 1-59 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1,11,17-18 and 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Ellis et al. (U.S Patent 6,256,687)

a. As per claim 1, Ellis discloses USB host system operationally coupled to a computing system with a main processor, comprising:

- a first processor (fig.4, 402), (fig.3, 302) that implements a USB driver (fig.1,210) without using the main processor (fig.1, 110) resources; (col.9, lines 6-13)
- a downstream USB port; (fig.1, 170)
- a communication area accessible both by the main processor and by the first processor such that the first processor interfaces with the main processor via the communication area using predefined records in pre-defined formats, wherein the main processor writes a data transfer request in the communication area in a pre-defined record format and the first processor schedules and completes the request via a USB host controller. (col.3, lines 35-67), (col.4,lines 1-67), (col.5, lines 1-22)

b. As per claim 11, Ellis discloses a USB host system operationally coupled to a computing system, comprising:

- a first processor (fig.4, 402), (fig.3, 302) that implements a USB driver (fig.1,210) without using the main processor (fig.1, 110) resources; (col.9, lines 6-13)
- a downstream USB port; (fig.1, 170)
- an interface between (fig.2,170) the first processor and second processor that provides a high-level USB pipe view of a USB system to an application program running on the second processor in the computing system. (col.5, lines 9-22)

c. As per claim 17, Ellis discloses information processing system comprising:

- a first process processor; (fig.1, 110)
- a data transfer host system comprising a second processor implementing a first data transfer driver managing a data transfer between the said first processor and a device; a data transfer port for connecting a device to the said data transfer host system; and an interface with the first processor that provides a high-level view of the data transfer process to the first processor. (col.3, lines 35-67), (col.4, lines 1-67), (col.5, lines 1-22), (col.5, lines 9-22)

d. As per claim 18, Ellis discloses interface (fig.1, 170) uses a memory area that can be accessed by both the said first processor and the second processor.

e. As per claim 21, Ellis discloses the first processor interfaces the data transfer host system via a standard microprocessor bus(fig.1, 115).

f. As per claim 22, Ellis discloses a hub is used to provide multiple ports for connecting a plural of devices. (col.1, lines 25-31)

e. As per claim 23, Ellis discloses first processor contains a second data transfer driver capable of managing the same data transfer and a data transfer request by the first processor to the second data transfer driver is carried out by the data transfer host system. (col.3, lines 35-67), (col.4, lines 1-67), (col.5, lines 1-22)

5. Claims 24-32, 38-43 and 46-59 are rejected under 35 U.S.C. 102(e) as being anticipated by Larky et al. (U.S Patent 6,389,495)

a. As per claim 24, Larky discloses a USB host comprising:

- a first processor implementing a function of a USB system; (col.4, lines 26-44)
- a downstream USB port; (fig.1,106)
- a memory accessible by the first processor and a second processor external to the USB host, where a first area of the memory with first predetermined format is used for a first type of transfer, and a second area of the memory with a second predetermined format is used for a second type of transfer. (col.7, lines 21-67), (col.8, lines 1-18), (col.9, lines 26-35)

b. As per claim 25, Larky discloses a hub (fig.1, 130) connected to the downstream USB port so that multiple devices can be connected to the system.

c. As per claim 26, Larky discloses the memory is connected to both the first processor and the second processor via a standard microprocessor bus interface. (fig.1, 106)

d. As per claims 27 and 55, Larky discloses a third area of the memory with a third predetermined format is used for reporting device connection, enumeration and removal to the second processor. (col.4, lines 26-44), (col.5, lines 15-48)

e. As per claim 28, Larky discloses third area is in a part of the said memory which is read-only to the second processor. (fig.1, 122)

f. As per claims 29 and 56, Larky discloses a fourth area of the memory with a fourth predetermined format is used for sending a USB command to the said USB host. (col.6, lines 5-25)

g. As per claims 30 and 57, Larky discloses the starting address of each memory area for a transfer is used to identify the transfer. (col.8, lines 19-67)

h. As per claim 31, Larky discloses the second processor allocates the size of a memory area for a transfer to fit the need of the transfer. (col.8, lines 19-67), (col.9, lines 1-25)

i. As per claim 32, Larky discloses the second processor allocates the number of the said areas to fit the need of a transfer. (col.8, lines 19-67)

j. As per claim 38, Larky discloses second processor writes a transfer request in a said area in the memory and notifies the first processor with an interrupt signal. (col.8, lines 51-67)

k. As per claim 39, Larky discloses the first processor writes the status or data of a transfer into a said area in the memory and notifies the said second processor with an interrupt signal. (col.8, lines 51-67)

l. As per claim 40, Larky discloses a single format of the said second area implements isochronous, interrupt and bulk transfers. (col.8, lines 51-67)

m. As per claim 41, Larky discloses a USB host comprising:

- a first processor implementing a function of a USB system; (col.4, lines 22-44)
- a downstream USB port; (fig.1, 106)
- a memory accessible (fig.3, 104, 126) by both the first processor (fig.1, 116) and second processor(fig.1, 120) external to the said USB host, whereby the said second processor initiates a USB transfer by writing a

transfer request, and data for the said transfer, if there is any, into a first area in the said memory, and the said first processor carries out the transfer, and writes the status of the said transfer, and data from the said transfer, if there is any, into a second area in the said memory. (col.7, lines 21-67), (col.8, lines 1-18), (col.9, lines 26-35)

n. As per claim 42, Larky discloses a hub (fig.1, 130) is connected to the downstream USB port so that multiple devices can be connected to the system.

o. As per claims 43 and 54, Larky discloses the memory is connected to both the first processor and the second processor via a standard microprocessor bus interface. (fig.1, 106)

p. As per claim 46, Larky discloses the second processor runs an operating system that supports USB and USB transfer request by the said second processor to USB driver on the second processor on the second processor is carried out by the USB host. (col.4, lines 22-44)

q. As per claim 47, Larky discloses the first processor carries out the transfer, and writes the status of the said transfer, and data from the said transfer, if there is any, into a second area in the said memory, the said USB host generates an interrupt signal to the said second processor to notify the said second processor. (col.3, lines 61-67), (col.4, lines 1-67), (col.5, lines 1-26)

r. As per claim 48, Larky discloses second processor initiates a USB transfer by writing a transfer request, and data for the said transfer, if there is any, into a first area in the said memory, the said second processor generates an interrupt signal

to the said USB host to notify the said USB host. (col.3, lines 61-67), (col.4, lines 1-67), (col.5, lines 1-26)

s. As per claim 49, Larky discloses a USB host system operationally coupled to a computing system with a main processor, comprising a processor (fig.1,120) that interfaces with the main processor (fig.1, 116) via a communication area using predefined records in pre-defined formats, wherein the main processor writes a data transfer request in the communication area in a pre-defined record format and the processor schedules and completes the request via a USB host controller. (col.4, lines 26-44)

t. As per claim 50, Larky discloses the processor returns status (fig.5, 506) and data to the main processor based on a request from the main processor. (col.9, lines 26-47)

u. As per claim 51, Larky discloses the communication area is a dual port memory (fig.6, 608) with plural registers.

t. As per claim 52, Larky discloses the main processor may poll the communication area and/or be notified by an interrupt generated by the processor. (col.8, lines 51-64)

v. As per claim 53, Larky discloses the communication area is divided into a first area with a predefined format for a first type of transfer, and a second area with a second predefined format for a second type of transfer. (col.4, lines 26-44), (col.8, lines 18-64)

w. As per claim 58, the main processor may allocate the dual port memory areas for a transfer. (col.9, lines 26-48)

x. As per claim 59, the dual port memory may implement isochronous, interrupt and /or bulk transfers. (col.8, lines 51-67)

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madden et al. (U.S Patent 6,393,493) in view of Ellis et al. (U.S Patent 6,256,687)

a. As per claim 2, Madden discloses the communication area is a dual port memory. (fig.2, 144)

b. As per claim 3, Madden discloses the communication area consists of multiple FIFO registers. (fig.7, 456)

c. As per claim 4, Madden discloses an interrupt polled from a USB interrupt pipe is converted to an interrupt signal to the Main Processor. (col.3, lines 21-30)

d. As per claim 5, Madden discloses the main processor interfaces the host system via a standard microprocessor bus. (fig.2, 154), (col.3, lines 21-30)

e. As per claim 6, Madden discloses a hub is used to provide multiple downstream USB ports. (col.5, lines 35-41)

f. As per claim 7, Madden discloses data in the communication area is directly sent out on a USB bus. (col.6, lines 6-8)

g. As per claim 8, Madden discloses where data received from the USB bus are written directly in the communication area. (col.4, lines 45-54)

h. As per claim 9, Madden discloses where the USB host system provides a USB function to the main processor. (fig.2, 154), (col.5, lines 31-37)

i. As per claim 10, Madden discloses where the USB host stem is used to provide a USB host function to the said second processor which runs an operating system supporting USB, by intercepting call to USB driver in the operating system. (col.6, lines 35-55, also see abstract)

Madden discloses the limitations as claimed as claims 2-10 as above except Madden fails to discloses the limitations as claimed as claim 1. However, Ellis discloses a) a first processor (fig.4, 402), (fig.3, 302) that implements a USB driver (fig.1,210) without using the main processor (fig.1, 110) resources; (col.9, lines 6-13). b) a communication area accessible both by the main processor and by the first processor such that the first processor interfaces with the main processor via the communication area using predefined records in pre-defined formats, wherein the main processor writes a data transfer request in the communication area in a pre-defined record format and the first processor schedules and completes the request via a USB host controller. (col.3, lines 35-67), (col.4,lines 1-67), (col.5, lines 1-22)

It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate Ellis's teaching into Madden's method to have the USB host system with its own processor runs the USB driver and host controller driver so as to be better managing and servicing USB devices from the main processor and so as to be compatible with the latest advancements in the communication system.

8. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Madden et al. (U.S Patent 6,393,493) in view of Ellis et al. (U.S Patent 6,256,687)

a. As per claim 12, Madden discloses where said interface uses a memory that can be accessed by both the first processor and the second processor. (col.4, lines 45-54 and 65-67)

b. As per claim 13, Madden discloses the second processor interfaces the host system via a standard microprocessor bus. (fig.2, 154), (col.3, lines 21-30)

c. As per claim 14, Madden discloses a hub is used to provide multiple downstream USB ports. (col.5, lines 35-41)

d. As per claim 15, host system is used t provide a USB host function to the second processor. (fig.2, 154), (col.5, lines 31-37)

e. As per claim 16, the host system is used to provide a USB host function to the said second processor which runs an operating system supporting a USB driver, and USB transfer request by the said second processor intercepting calls to the USB driver in the operating system. (col.6, lines 36-55), (also see abstract)

Madden discloses the limitations as claimed as claims 12-16 as above except Madden fails to discloses the limitations as claimed as claim 11. However, Ellis discloses a) a first processor (fig.4, 402), (fig.3, 302) that implementing a function for managing a USB host controller with or without an operating system running on the computing system. b) an interface (fig.2, 170) between the first processor and a second processor that provides a high-level USB pipe view of a USB system to an application program running on the second processor in the computing system. (col.5, lines 9-22)

It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate Ellis's teaching into Madden's method to have the USB host system with its own processor runs the USB driver and host controller driver so as to be better managing and servicing USB devices from the main processor and so as to be compatible with the latest advancements in the communication system.

9. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis et al. (U.S Patent 6,256,687) in view of Mitra (U.S Patent 5,594,894)

f. As per claim 19 and 20, Ellis discloses the limitations as claimed as claims 17-23 as above except Ellis fails to disclose processor is used to reduce the number of interrupt and to reduce the frequency of interrupts. However, Mitra discloses reduce the interrupts by reducing the frequency of the interruptions. (col.2, lines 64-67)

It would have been obvious one having ordinary skills in the art at the time the invention was made to incorporate Mitra's teaching into Ellis's method to the processor to reduce the interrupts by reducing the frequency of the interruptions so as to be more efficiency and accuracy to the system.

g. As per claims 33-37 and 44-45 Larky fails to discloses starting address are being different, same or fixed location of memory, Larky does teach the configuration data load into the device RAM. (col.8, lines 57-60)

Examiner take Official Notice of the starting address being located in a different part of memory is well known in the art. It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate the starting address being located in a different part of memory into Larky's method so as to increase the flexibility of the system.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7249 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

Dec.23, 2002

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100